I2C Master Controller

AXI4-Lite I2C Master

IP Core · i2c

RUNX-PB-I2C-001 · 2026-08-11 **Product Brief**

Introduction

The RunX I2C Master Controller is an AXI4-Lite peripheral.

Features

- AXI4-Lite slave interface
- 32-word TX and RX FIFOs
- Twelve 32-bit registers at 0x00–0x2C, with read-only VERSION, BUILD_DATE and CLK_INFO identification registers.
- Standard-mode and Fast-mode bit rates, 100 kHz–800 kHz, elaborated from SYS_CLK / I2C_CLK.
- Four-phase bit engine with a programmable clock-stretch timeout and a dedicated sticky TIMEOUT flag.
- Multi-master arbitration: a transaction aborts without a STOP if the bus reads back low while the core drove high.
- Repeated START (Sr) via CTRL.REPEAT_START, suppressing the closing STOP between back-to-back transactions.
- Separate sticky NACK, TIMEOUT and ARB_LOST error flags, OR'd into STATUS.ERROR.
- Interrupt-on-value match, independently maskable from CTRL.INT_EN.
- Vendor-agnostic RTL — no vendor primitives instantiated; DEVICE selects inference hints for Xilinx/AMD, Altera/Intel, Lattice, Microchip or an ASIC target.

IP Facts					
Core Specifics					
Product Name	I2C Master Controller				
IP Identifier	RUNX-PL-I2C-v1				
IP Version	v1.0.0				
Bus Interface	AMBA AXI4-Lite (32-bit slave)				
Release Status	[Engineering / Pre-Release / Production]				
Verification Status	[e.g., Verified with RunX VIP across parameter sweeps]				
Validation Status	[e.g., Validated on industrial hardware]				
Provided with Core					
Delivery Format	[RTL source · IEEE-1735 encrypted per vendor]				
Vendor Support	[AMD/Xilinx · Intel/Altera · Microchip]				
Constraints	[XDC · SDC]				
Simulation	[e.g., SystemVerilog-2017 testbench]				
Supported SW driver	[e.g., Bare-metal C driver included]				
Document					
Document Number	RUNX-PB-I2C-001				
Document Revision	[Rev A / Draft]				
Date	2026-08-11				
Synthesis & Implementation					
Vendor	**LUT**	**FF**	**DSP**	**BRAM**	**Fmax**
Xilinx	395	375	0	1	256 MHz
Altera	553	399	0	2 048 b	317 MHz
Lattice	~620	~462	0	0	288 MHz
Microchip	[—]	[—]	[—]	[—]	[—]
Support					
info@run-x.com · www.run-x.com					

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SECTION

Introduction

1.1 Overview

1.2 Key Features

1.3 Target Applications

1.4 Supported Device Families

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SECTION

Functional Overview

2.1 Block Diagram (simplified)

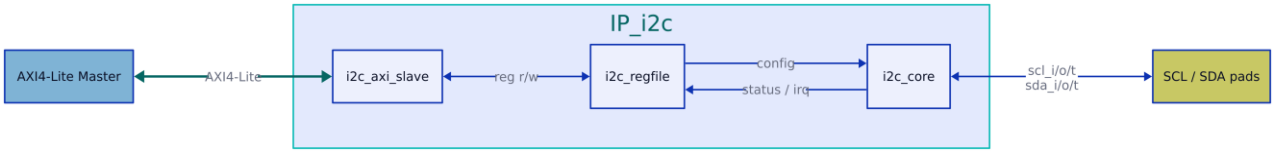

Figure 2.1.1 — IP_i2c top-level structure and external connections.

2.2 Port List (names/widths only)

Port	Dir	Width
s_axi_aclk	in	1
s_axi_aresetn	in	1
s_axi_awaddr	in	8
s_axi_awprot	in	3
s_axi_awvalid / s_axi_awready	in / out	1 / 1
s_axi_wdata	in	32
s_axi_wstrb	in	4
s_axi_wvalid / s_axi_wready	in / out	1 / 1
s_axi_bresp / s_axi_bvalid / s_axi_bready	out / out / in	2 / 1 / 1
s_axi_araddr	in	8
s_axi_arprot	in	3
s_axi_arvalid / s_axi_arready	in / out	1 / 1
s_axi_rdata	out	32
s_axi_rresp / s_axi_rvalid / s_axi_rready	out / out / in	2 / 1 / 1
sda	inout	1
scl	inout	1
int_o	out	1

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Performance Summary

3.1 Resource Utilization (headline)

Vendor / part	LUT/ALUT	Registers	Memory	DSP
AMD/Xilinx (Kintex-7, xc7k70tfbv676-1)	388	375	1 BRAM tile	0
Intel/Altera (Agilex 3, A3CY135BM16AE6S)	553	399	2048 mem bits	0

3.2 Maximum Frequency (Fmax, headline)

Vendor	Reported WNS (@200MHz)	Fmax
AMD/Xilinx	+1.107 ns	256.2 MHz
Intel/Altera	+1.847 ns	317.2 MHz
Lattice	+1.547 ns	288 MHz

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Licensing & Ordering

4.1 Licensing Options

The core is licensed per design or per project. A design licence covers use in one named end product; a project licence covers unlimited designs within one organisation for the licence term. Both include the RTL sources, the C driver, the constraint template and the Product User Guide.

The I2C Verification IP is a separate product and is not included in either licence tier.

4.2 Deliverables

- RTL sources — i2c_master_top.sv and its four sub-modules, plus the transparent Verilog-2001 wrapper IP_i2c.v
- driver/i2c_master.c / .h — bare-metal C driver and public API header
- constraints/i2c.xdc — timing constraint template
- sim/scripts/ — xsim and Questa run scripts for the testbench and VIP flows
- docs/ — the Product User Guide, block diagrams and WaveDrom timing sources

4.3 Contact & Support

Technical support is provided by RunX Technology Inc. Include the IP identifier, the RTL version and the document number from page 1 of this brief when raising a query, together with the target device and toolchain version. Email — info@run-x.com. Web — www.run-x.com.

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Revision History

5.1 Document Revision History

The following table lists the revision history of this document. Each entry names the sections that were added, changed, or removed, and the IP Version column records the core release that revision of the document describes.

Date	Doc Rev.	IP Version	Description of Change
2026-08-11	[D]	v1.0.0	• [Section N.n — summarise what was added, changed, or removed.] • [One bullet per edited section, named, so two revisions can be diffed at a glance.]
2026-08-11	[C]	v1.0.0	• [Added Section N.n — <title>.] • [Updated Table N-n to cover <what changed>.] • [Removed <what was dropped> from Section N.n.]
2026-08-11	[B]	v1.0.0	• [Editorial revision — no technical content changed.]
2026-08-11	[A]	v1.0.0	Initial RunX release.

5.2 IP Version History

The following table lists the release history of the IP core itself. Document revisions and core releases do not track in lockstep — one core release may be described by several document revisions, and an editorial document revision may describe no new core release at all.

Release Date	IP Version	Release Status	Change Summary
2026-08-11	v1.0.0	[Production]	• [Functional change — new feature, parameter, or port.] • [Bug fix — reference the errata item it closes.]
2026-08-11	v1.0.0	[Pre-Release]	• [Interface change — record any backward incompatibility here.] • [Performance or resource change, with the numbers it supersedes.]
2026-08-11	[v1.0.0]	[Engineering]	Initial release of the core.